Amendments to the Claims

Please amend claims 1,2, 11, 12, 22, and 31. The currently pending claims after amendment are listed below.

1. (Currently Amended) A digital data processing device, comprising:

at least one processor;

a memory;

a first cache for temporarily holding portions of said memory, said first cache containing a plurality of addressable associativity sets, each associativity set containing one or more respective cache lines and corresponding to a respective first cache subset of a plurality of discrete first cache subsets of addresses for accessing said first cache; and

a second cache for temporarily holding portions of said memory, said second cache containing a plurality of addressable associativity sets, each associativity set containing one or more respective cache lines and corresponding to a respective second cache subset of a plurality of discrete second cache subsets of addresses for accessing said second cache;

wherein each said associativity ~~sets~~ set of said first cache and each said associativity ~~sets~~ set of said second cache ~~correspond to~~ is contained in a respective congruence group of a plurality of congruence groups, each congruence group containing a respective plurality of associativity sets of said first cache and a respective plurality of associativity sets of said second cache;

wherein addresses of the first cache subset corresponding to each respective associativity set of said first cache are allocated among each of the plurality of second cache subsets corresponding to respective associativity sets in said second cache within the same congruence group as the respective associativity set of said first cache.

2. (Currently Amended) The digital data processing device of claim 1, wherein addresses of the first cache subset corresponding to each respective associativity set of said first cache are allocated among each of the plurality of second cache subsets corresponding to respective associativity sets in the second cache within the same congruence group using a hashing function of at least some address bits other than address bits used to determine the respective associativity set.

3. (Original) The digital data processing device of claim 2, wherein said hashing function is a modulo-N function, where N is the number of associativity sets of said second cache in said congruence group.

4. (Original) The digital data processing device of claim 1, wherein each said congruence group contains M associativity sets of said first cache and N associativity sets of said second cache, wherein the greatest common factor of M and N is one.

5. (Original) The digital data processing device of claim 1, wherein data is not duplicated in said first and second caches.

6. (Original) The digital data processing device of claim 1, wherein said first cache is at a higher level than said second cache.

7. (Original) The digital data processing device of claim 6, wherein said second cache is a victim cache of said first cache.

8. (Original) The digital data processing device of claim 6, wherein said digital data processing device comprises a third cache, said third cache being at a level higher than said first cache and said second cache.

9. (Original) The digital data processing device of claim 1, wherein said first and second caches are addressable using real memory addresses.

10. (Original) The digital data processing device of claim 1, wherein each said associativity set in said first cache contains a respective plurality of cache lines, and each said associativity set in said second cache contains a respective plurality of cache lines.

11. (Currently Amended) An integrated circuit chip for digital data processing, comprising:

at least one processor core;

first cache accessing logic for accessing a first cache, said first cache temporarily holding portions of a memory, said first cache accessing logic determining an associativity set of said first cache which corresponds to an input address generated by said processor core from among a plurality of associativity sets of said first cache, each associativity set containing one or more respective cache lines, wherein a respective first cache subset of input addresses of a plurality of discrete first cache subsets of input addresses corresponds to each associativity set of said plurality of associativity sets of said first cache; and

second cache accessing logic for accessing a second cache, said second cache temporarily holding portions of said memory, said second cache accessing logic determining an associativity set of said second cache which corresponds to said input address generated by said processor core from among a plurality of associativity sets of said second cache, each associativity set containing one or more respective cache lines, wherein a respective second cache subset of input addresses of a plurality of discrete second cache subsets of input addresses corresponds to each associativity set of said plurality of associativity sets of said second cache;

wherein each said associativity ~~sets~~ set of said first cache and each said associativity ~~sets~~ set of said second cache ~~correspond to~~ is contained in a respective congruence group of a plurality of congruence groups, each congruence group containing a respective plurality of associativity sets of said first cache and a respective plurality of associativity sets of said second cache;

wherein input addresses of the first cache subset corresponding to each respective associativity set of said first cache are allocated among each of the plurality of second cache subsets corresponding to respective associativity sets in said second cache within the same congruence group as the respective associativity set of said first cache.

12. (Currently Amended) The integrated circuit chip of claim 11, wherein input addresses of the first cache subset corresponding to each respective associativity set of said first cache are allocated among each of the plurality of second cache subsets corresponding to respective associativity sets in said second cache within the same congruence group using a hashing function of at least some address bits other than address bits used to determine the respective associativity set.

13. (Original) The integrated circuit chip of claim 12, wherein said hashing function is a modulo-N function, where N is the number of associativity sets of said second cache in said congruence group.

14. (Original) The integrated circuit chip of claim 11, wherein each said congruence group contains M associativity sets of said first cache and N associativity sets of said second cache, wherein the greatest common factor of M and N is one.

15. (Original) The integrated circuit chip of claim 11, wherein data is not duplicated in said first and second caches.

16. (Original) The integrated circuit chip of claim 11, wherein said first cache is at a higher level than said second cache.

17. (Original) The integrated circuit chip of claim 16, wherein said second cache is a victim cache of said first cache.

18. (Original) The integrated circuit chip of claim 11, wherein said first and second caches are addressable using real memory addresses.

19. (Original) The integrated circuit chip of claim 11, wherein each said associativity set in said first cache contains a respective plurality of cache lines, and each said associativity set in said second cache contains a respective plurality of cache lines.

20. (Original) The integrated circuit chip of claim 11, wherein said chip includes at least one of said first cache and said second cache.

21. (Original) The integrated circuit chip of claim 11, wherein said chip includes a plurality of processor cores, said plurality of processor cores sharing said first and second caches.

22. (Currently Amended) A method of operating cache memory in a digital data processing device, comprising the steps of:

responsive to an input address, determining an associativity set of a first cache which corresponds to said input address from among a plurality of associativity sets of said first cache, each associativity set containing one or more respective cache lines, wherein a respective first cache subset of input addresses of a plurality of discrete first cache subsets of input addresses corresponds to each associativity set of said plurality of associativity sets of said first cache;

responsive to said step of determining an associativity set of a first cache, determining whether the associativity set determined by said step of determining an associativity set of a first cache contains data corresponding to said input address;

responsive to said input address, determining an associativity set of a second cache which corresponds to said input address from among a plurality of associativity sets of said second cache, each associativity set containing one or more respective cache lines, wherein a respective second cache subset of input addresses of a plurality of discrete second cache subsets of input addresses corresponds to each associativity set of said plurality of associativity sets of said second cache;

responsive to said step of determining an associativity set of a second cache, determining whether the associativity set determined by said step of determining an associativity set of a second cache contains data corresponding to said input address;

wherein each said associativity ~~sets~~ set of said first cache and each said associativity ~~sets~~ set of said second cache ~~correspond to~~ is contained in a respective congruence group of a plurality of congruence groups, each congruence group containing a respective plurality of associativity sets of said first cache and a respective plurality of associativity sets of said second cache;

wherein, for each subset pair (S1, S2) consisting of a subset S1 of first cache input addresses corresponding to ~~each respective~~ an associativity set of said first cache within a congruence group C ~~are allocated among the plurality of~~ and a subset S2 of second cache input addresses corresponding to an associativity ~~sets in~~ set of said second cache within the same congruence group ~~as the respective associativity set of said first cache~~ C, the intersection of the two subsets S1 and S2 of the subset pair is a non-empty set of input addresses.

23. (Original) The method of claim 22, wherein addresses corresponding to each respective associativity set of said first cache are allocated among the plurality of associativity sets in the second cache within the same congruence group using a hashing function of at least some address bits other than address bits used to determine the respective associativity set.

24. (Original) The method of claim 23, wherein said hashing function is a modulo-N function, where N is the number of associativity sets of said second cache in said congruence group.

25. (Original) The method of claim 22, wherein each said congruence group contains M associativity sets of said first cache and N associativity sets of said second cache, wherein the greatest common factor of M and N is one.

26. (Original) The method of claim 22, wherein data is not duplicated in said first and second caches.

27. (Original) The method of claim 22, wherein said first cache is at a higher level than said second cache.

28. (Original) The method of claim 27, wherein said second cache is a victim cache of said first cache.

29. (Original) The method of claim 22, wherein said first and second caches are addressable using real memory addresses.

30. (Original) The method of claim 22, wherein each said associativity set in said first cache contains a respective plurality of cache lines, and each said associativity set in said second cache contains a respective plurality of cache lines.

31. (Currently Amended) A digital data processing device, comprising:

at least one processor;

a memory;

a first cache for temporarily holding portions of said memory, said first cache containing a plurality of addressable associativity sets, each associativity set containing one or more respective cache lines; and

a second cache for temporarily holding portions of said memory, said second cache containing a plurality of addressable associativity sets, each associativity set containing one or more respective cache lines;

wherein each said associativity set of said first cache corresponds to a respective first cache subset containing a respective plurality of addresses of data storable in the associativity set of said first cache, and each said associativity set of said second cache corresponds to a respective second cache subset containing a respective plurality of addresses of data storable in the associativity set of said second cache;

wherein addresses contained in the first cache subset corresponding to each respective associativity set of said first cache are allocated among each of a respective plurality of second cache subsets corresponding to respective associativity sets in said second cache;

wherein addresses contained in the second cache subset corresponding to each respective associativity set of said second cache are allocated among each of a respective plurality of first cache subsets corresponding to respective associativity sets in said first cache.

32. (Currently Amended) The digital data processing device of claim 31, wherein addresses contained in the first cache subset corresponding to each respective associativity set of said first cache are allocated among each of the plurality of ~~associativity sets in the second cache~~ second cache subsets using a hashing function of at least some address bits other than address bits used to determine the respective associativity set of said first cache.

33. (Original) The digital data processing device of claim 32, wherein said hashing function is a modulo-N function, where N is the number of associativity sets of said second cache to which addresses in an associativity set of said first cache are allocated.

34. (Original) The digital data processing device of claim 31, wherein data is not duplicated in said first and second caches.

35. (Original) The digital data processing device of claim 31, wherein said first cache is at a higher level than said second cache.

36. (Original) The digital data processing device of claim 35, wherein said second cache is a victim cache of said first cache.